PROGRAMMABLE CLOCK MULTIPLICATION USING DELAY LOCKED LOOP

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Abstract

In this paper a programmable clock multiplier based on Delay Locked Loop (DLL) is proposed. It does not require any L-C tank circuit or ring oscillator. Although it requires a clean reference signal it has several advantages over conventional Phase Locked Loop (PLL) based clock multiplication in terms of stability, power consumption, jitter performance and ease to design. The operating frequency range of DLL is 170 MHz to 252 MHz. The proposed clock multiplier is programmable with multiplication factor of 1X, 2X, 4X and hence can generate clock of frequency range 170 MHz to 1 GHz with 50 % duty cycle. The proposed circuit is simulated in SPICE at 180 nm technology node and 1.8 V power supply with a reference signal of 200 MHz and output signal is shown with various multiplication factor. The power consumption in each case is less than 10 mw.

Keywords:

I.INTRODUCTION

With the advancement of nanometer scale process in CMOS technology, the demand for high performance VLSI system continues to grow exponentially. These advances have led to the increase in clock frequencies in synchronous circuits as well as in the local oscillators of communication system. At these high frequencies the clock signals need to be very stable in-order to satisfy the timing requirements in synchronous circuits and also to reduce the close-in phase noise in local oscillators. Due to interconnection problem it is difficult to launch a high frequency signal to the chip, thus making a requirement for an on chip clock multiplier in microprocessors and in high speed serial I/O link. DLL based clock multipliers offer several advantages over conventional PLL based clock multipliers. A DLL is a 1st order system and hence inherently stable, unlike PLL which is a higher order system requiring complex loop filter. This also makes DLL easy to design and integrate on chip. DLL does not have the problem of jitter accumulation over many clock cycles, which is present in PLL and, thus results in low phase noise and stable output signal[1]. Recently, several DLL-based clock multipliers for high speed circuits and local oscillator have been proposed to overcome the difficulty of frequency multiplication with DLLs and utilize the several inherent advantage of DLLs over PLLs [2-6]. Other application of DLL includes clock skew reduction in distribution networks [7], digital testing of timing sensitive parameters [8] and data recovery in high speed I/O interfaces [9]. In this paper a programmable clock multiplier is presented at 180 nm technology with multiplication factor of 1X, 2X and 4X depending on the external digital signals. The proposed clock multiplier can generate frequencies as high as 1 GHz and hence can be used in various applications.

II.ARCHITECTURE

A. Conventional Architecture

Fig.(1) shows the block diagram of DLL. It consists of a phase detector (PD), a charge pump (CP), a loop filter (LP),Voltage Controlled Delay Line (VCDL). The VCDL consists of several stages of delay cell, as shown. The PD unit generates UP or DN pulse depending on

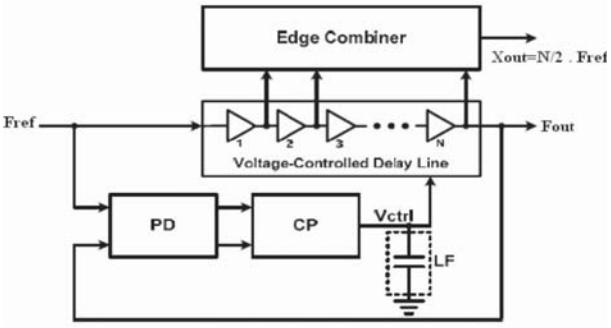


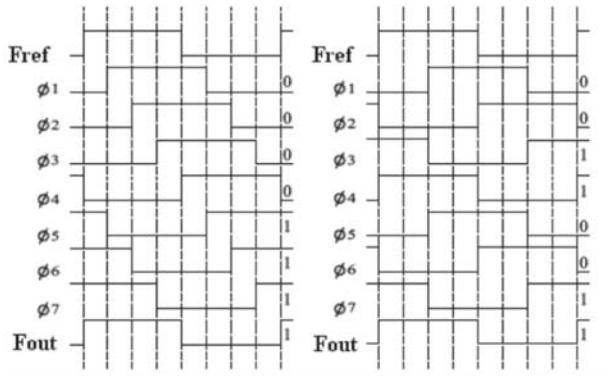
Fig. 1. Block diagram of Conventional DLL based frequency multiplier

the phase error between Fref and Fout. CP unit utilizes these pulses in order to pump in or pump out charge (and hence voltage) from the loop filter capacitor, thereby generating a control voltage Vctrl for VCDL. When DLL is locked Vctrl is constant (with small ripples) and Fref and Fout are exactly in phase. In locked state the outputs of delay cells of VCDL generate a family of waveforms whose rising edges are equally phased within one reference period of reference signal. The edge combiner utilizes these equally phased high frequency transition to generate a high frequency signal Xout. The maximum output frequency is given by. Xout = N/2 . Fref

where N, number of delay stages in VCDL, is even. The disadvantage of the conventional DLL based frequency multiplier is that the multiplication factor is fixed.

B. Locking range of DLL

The DLL may suffer from harmonic locking or false locking over wide operating range. Fig.(2) shows multiphase output waveform of an eight stage VCDL with correct and falsely



(a) (b)

Fig. 2. (a).correctly locked (b) falsely locked

C. Proposed Architecture

Fig. (3) shows the architecture of proposed DLL based programmable clock multiplier. The frequency multiplier part consists of additional phase selector and glitch generator locked DLL. In order to overcome incorrect locking problem, the maximum delay time and the minimum delay time , of VCDL have got an upper and a lower boundary given by the following relations [10]:

$$0.5\,T_{ref} < T_{VCDLMIN} < T_{ref} \quad (1)$$

$$T_{ref} < T_{VCDLMAX} < 1.5\,T_{ref} \quad (2)$$

where T_{ref} is the period of input reference signal. From the above relations, the range of stuck free clock period should satisfy following relation.

$$MAX(T_{VCDLMIN}, 2/3\,xT_{VCDLMAX}) < T_{ref} < MIN(T_{VCDLMAX}, 2xT_{VCDLMIN}) \quad (3)$$

If DLL does not satisfy these relations, it will fail to lock or falsely lock to two or more period.

A lock detector circuit [3] can also be used to detect and correct any false locking.

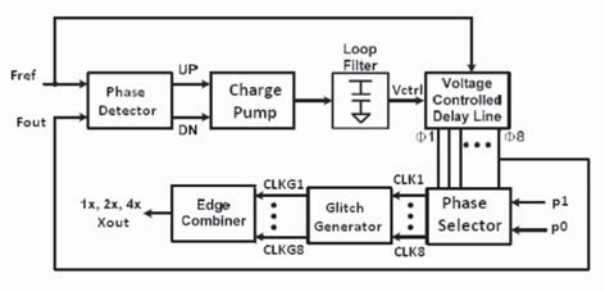


Fig. 3. Proposed DLL based programmable clock multiplier

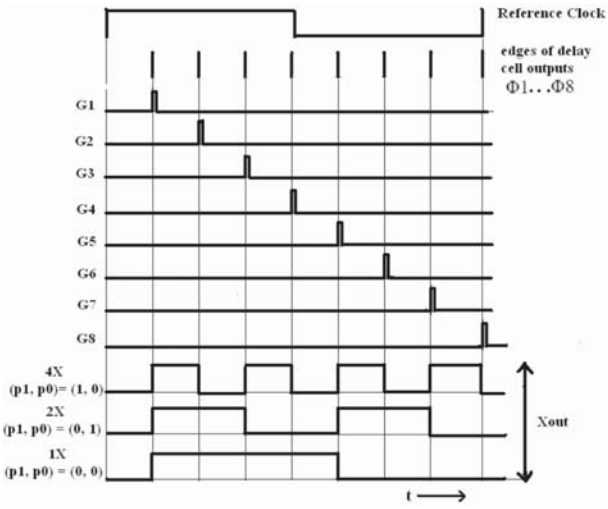


Fig. 4. Different cases for frequency multiplication

as compared to conventional architecture shown in Fig. (1). The VCDL consists of eight delay stages. There are two external digital signals, known as phase select signals (p1,p0), which are given to the phase selector. Depending on the values of these signals the phase selector selects and sends appropriate phases to the glitch generator and thereby enabling frequency multiplication of the reference signal with multiplication factor of 1X , 2X and 4X. Following are the output frequencies for different values of phase select signals (p1,p0)

When (p1, p0) = (0, 0) Xout=Fref (multiply by one)

When (p1, p0)=(0, 1) Xout=Fref x2 (multiply by two)

When (p1,p0)=(1, 0) Xout =Fref x 4 (multiply by four)

When (p1, p0) = (0, 0) the phase selector sends the phases Φ1 and Φ5 on two of its output lines (CLK(1…8)) to the glitch generator, the rest output lines remain grounded. The glitch generator generates corresponding glitches G1 and G5 on two of its output lines (CLKG(1…8)), with rest output lines remain grounded. The glitch G1 is used to generate a rising edge of the output signal and glitch G5 is used to generate the falling edge. Thus the output will have same frequency as that of the input.

When (p1, p0) = (0, 1) the phase selector sends the phases Φ1, Φ3, Φ5 and Φ7 to the glitch generator. The glitches G1and G5 are used to generate a rising edge of the output signal and glitches G3 and G7 are used to generate the falling edge. Thus the output will have twice frequency as that of the input.

When (p1, p0) = (1, 0) the phase selector sends all the phases (Φ1… Φ8) to the glitch generator. The glitches G1, G3, G5 and G7 are used to generate a rising edge of the output signal and glitches G2, G4, G6 and G8 are used to generate the falling edge. Thus the output will have four times the frequency as that of the input. Fig.(4) describes the above cases.

III.CIRCUIT DESCRIPTION

A. Phase Detector (PD)

Fig.(5) shows the phase detector incorporated in the proposed DLL based clock multiplier. It is a tri-state type PD and works on the principle of previous widely used PD with TSPC type D flip flop [11]. It removed the reset circuitry of PD in [11] but retained the advantage of better linearity range (from -2π to +2π) and almost negligible dead zone. It consists of minimum number of transistors and consumes less power.

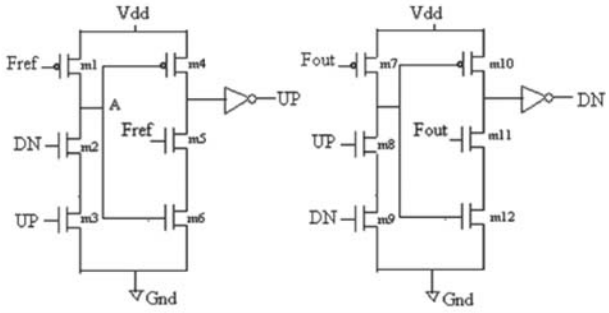
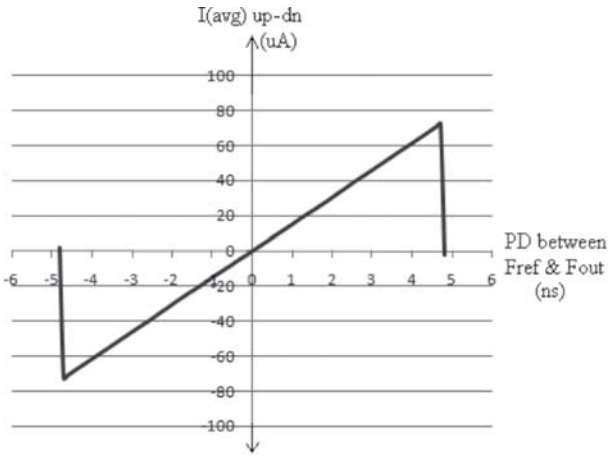


Fig. 5. PD in proposed DLL based clock multiplier

The characteristic of converting phase difference into loop filter current (80 uA) by incorporated PD is plotted with the help of simulation results obtained and is shown Fig.(6). We can see that characteristic is linear in region -5 ns to +5 ns, which corresponds to a phase difference of –2π to +2π for 200 MHz reference signal. The linearity range is seen to be slightly less than -2π to +2π, due to finite reset pulse width [12] as mentioned before. We see that even for a extremely small phase difference (order of ps) between the two inputs, there is net current flowing. Thus, dead zone of the PD is almost eliminated.



i g 6. Phasec har act er ist icso f PD

B. Charge Pump(CP)

The CP unit is responsible for generating necessary control voltage for the VCDL unit. The basic circuit for charge pump, consisting of two switched current sources is shown in Fig.(7). This circuit, if implemented, shows many non ideal effects like charge sharing, clock feed through and channel charge injection. These effects tend to produce ripples on the control voltage, resulting in phase noise and spurious tones at the output. Other design consideration for CP design is the UP/DN current mismatch and timing mismatch which should be kept minimum to reduce ripples on control voltage and minimize static phase error between Fref and Fout in locked state.

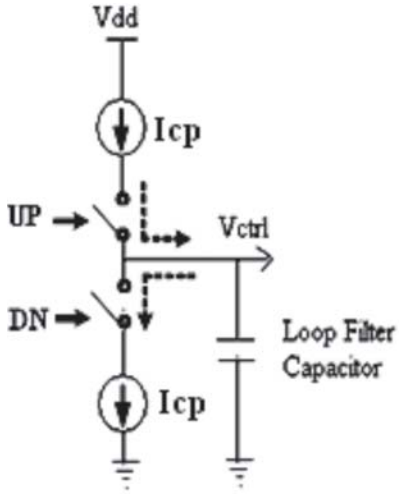


Fig. 7. Basic Charge Pump

(a) (b)

Fig. 8. (a) Block Diagram of CP (b) Pump up circuitChang and Kuo's model [13] provides the best solution for CP design. It eliminates the non-ideal effects completely by isolating the output node from the switching

transistors. At 180 nm technology node, this model shows significant difference in pump up and pump down currents due to Channel Length Modulation (CLM) effect. The CP of the proposed DLL, removes this current mismatch and is shown in

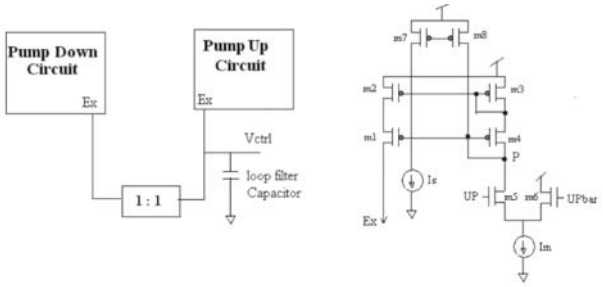


Fig. 8 (a). The pump up and pump down circuit are symmetric.

The pump up operation can be explained by Fig. 8(b). When UP is high a current of magnitude *Im-Is* is mirrored to node Ex and hence to the loop filter capacitor. A pull up circuit comprising of m7 and m8 is required to charge up the node P so that m4 and hence m1 is turned off as soon as UP goes low. The transistors m1,m2, m3 and m4 forms cascode configuration which increases the output impedance and hence suppresses CLM effects that become prominent at 180 nm technology node. On the negative side output swings are reduced. A low voltage wide swing current mirror is used for 1:1 current convertor. The charge pump is designed for a peak current of 80 uA.

C. *Voltage Controlled Delay Line (VCDL)*

The VCDL unit generates necessary delay depending on the control voltage applied to it. When the DLL is locked, the output of VCDL is delayed w.r.t input by exactly one period. The VCDL of the proposed DLL consists of eight stages of delay cell. The delay cell is based on current starved inverter configuration proposed by Johnson and Hudson [14]. It does not require any level conversion circuit as required by fully differential delay cell. It also has the advantage of being simple, occupying less chip area and consuming low power as the static power dissipation is zero [4].

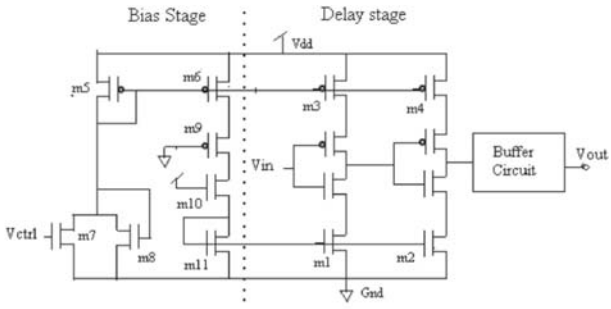


Fig. 9. Delay stage along with bias stage

Fig. (9) shows the delay cell used, along with the bias stage and is similar to that used by Chen *et al* [15]. The delay cell propagation delay depends on current source (m3, m4) and current sink (m1, m2). The bias stage and Vctrl controls the voltage to current sink and current source and thus controlling the delay. The larger the Vctrl the larger is the current and lesser is the delay provided. Measures to avoid false lock, as explained in the beginning, must be taken care of in the design. A buffer circuit (consisting of two static inverters) is connected at the output of delay cell in order to reduce rise time and fall time. The rise time and fall time should be kept minimum when DLL is used for application like frequency multiplication.

D. *Glitch generator*

Fig.(10) shows the glitch generator used in the programmable frequency multiplier. It generates a pulse of very short duration at the output when the CLK input undergoes a positive transition. Initially when clock CLK = 0, node X is pulled up to Vdd (m1 being a PMOS transistor. Therefore, initially (before rising edge of CLK) one of the inputs to the NAND gate is high (X) and other is low (CLK). This results in low output (CLKG=0). Now, when the rising edge of CLK arrives, there is a short period of time when both the inputs of NAND gate becomes high, causing CLKG to go high. This in turn activates m2 (m2 being NMOS), pulling down X and eventually CLKG goes low. The length of the pulse is controlled by delay of NAND gate and inverter.

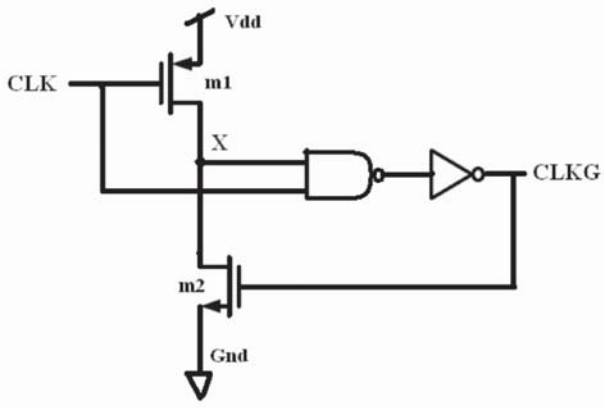


Fig. 10. Glitch generator

E. Phase Selector

Fig.(11) shows the basic unit of a phase selector. It is an implementation of 4 :1 (only three input considered here) MUX using pseudo-NMOS configuration. This unit is repeated eight times. The connections to A,B and C inputs are in accordance to table(1).

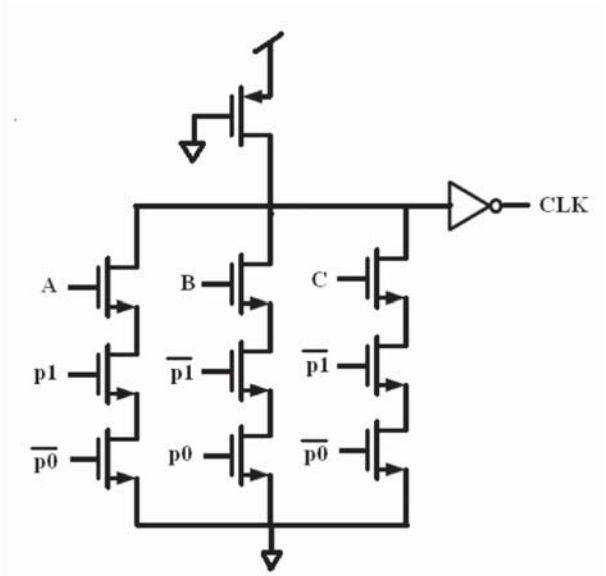


Fig. 11. Basic unit of phase selector *F. Edge Combiner*

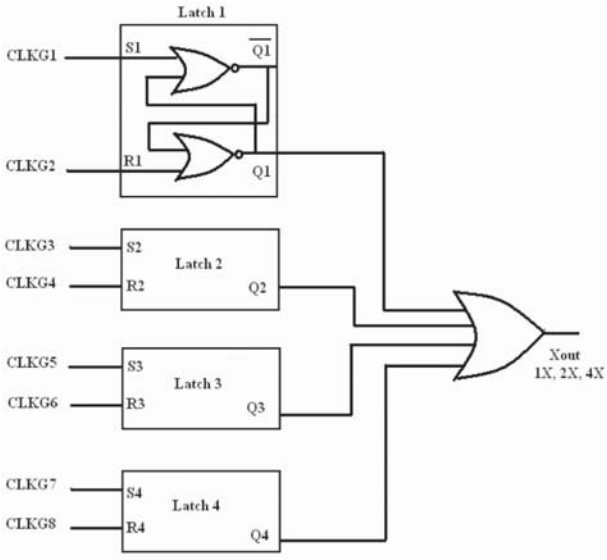


Fig. 12. Edge Combiner

Fig.(12) shows the edge combiner incorporated in the proposed programmable frequency multiplier. It consist of four S-R latches, followed by a four input OR gate. The output lines of glitch generator CLKG(1…8) are connected to the latches as shown. Consider the case when (p1, p0) = (1, 0). The A input of all the eight units of phase selector gets activated and therefore CLK(1…8) = Φ(1…8). These are passed to the glitch generator, which generates CLKG(1…8). These glitches are then passed to edge combiner. Thus the final output Xout is 4 times the input reference frequency and 50 % duty cycle. Other cases can be explained similarly

IV.SIMULATION RESULTS

All the units of DLL based programmable clock multiplier are interconnected and simulated for an input reference frequency of 200 MHz. The locking curve DLL obtained through simulations is shown in Fig. (13) along with waveforms of Fref and Fout. As seen, the lock time of the DLL is less than 300 ns. Fig. (14) shows the multiphase output waveform of all eight VCDL stages when DLL is locked. We can see that the output waveform of final stage (Fout) is in phase with the input reference waveform (Fref). Fig.(15-17) gives the output waveform Xout for different values of (p1, p0). A delay is observed between the start of Xout and Fref. This is because rising edge of output of first delay cell (which is delayed w.r.t Fref) is used to generate rising edge of Xout.

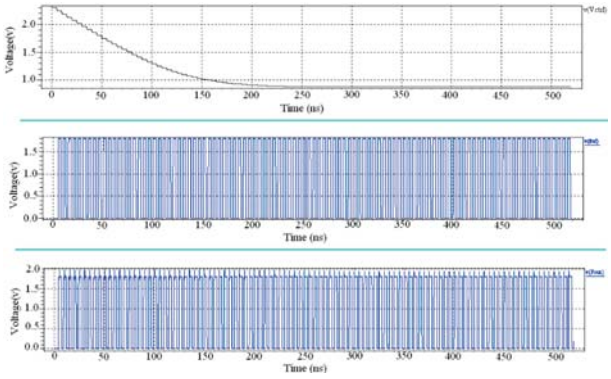


Fig. 13. output for locking curve, Fref, Fout

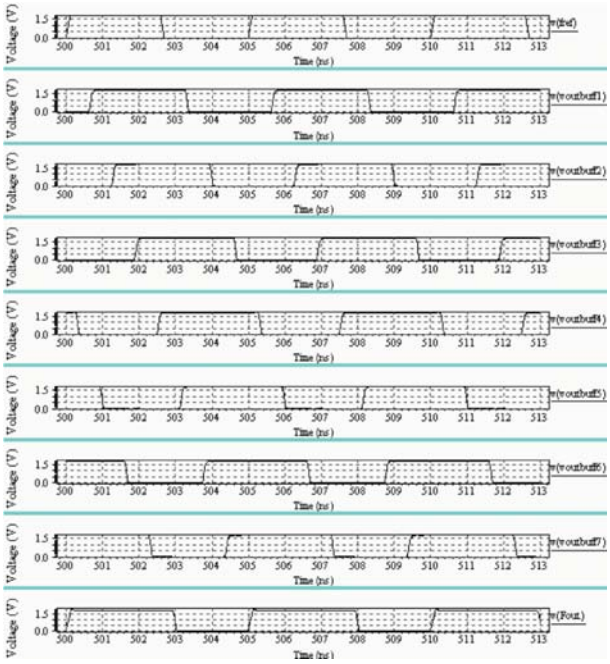


Fig. 14. Multiphase output when DLL is in locked state

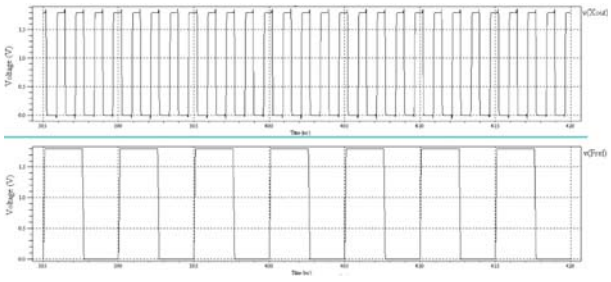


Fig.(15) Simulated output for (p1,p0)=(1, 0), Xout = 800 MHz @4X multiplication factor

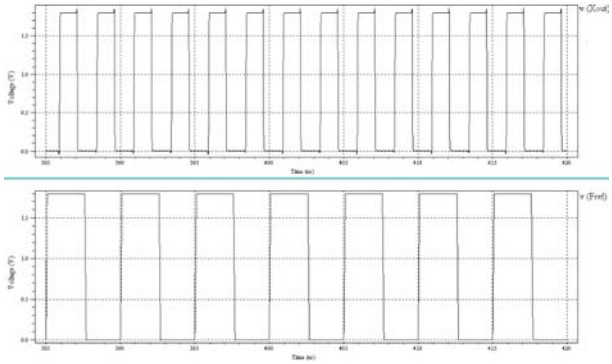


Fig. 16. Simulated output for (p1, p0) = (0, 1), Xout = 400 MHz @2X multiplication factor

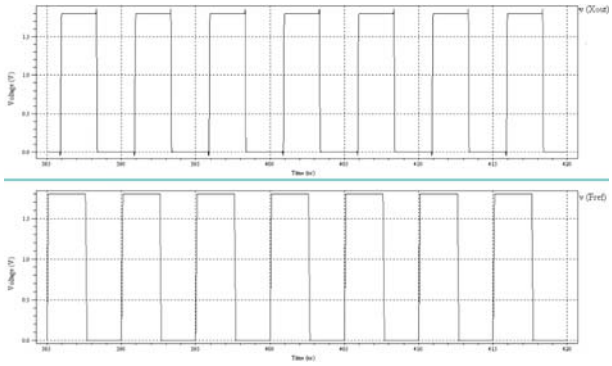


Fig. 17. Simulated output for (p1, p0) = (0, 0), Xout = 200 MHz @1X multiplication factor

Table 1. A,B,C input for various cases

	p1	p0	CLK1 (CLKG1)	CLK2 (CLKG2)	CLK3 (CLKG3)	CLK4 (CLKG4)	CLK5 (CLKG5)	CLK6 (CLKG6)	CLK7 (CLKG7)	CLK8 (CLKG8)
A	1	0	Φ1 (G1)	Φ2 (G2)	Φ3 (G3)	Φ4 (G4)	Φ5 (G5)	Φ6 (G6)	Φ7 (G7)	Φ8 (G8)
B	0	1	Φ1 (G1)	Φ3 (G3)	Φ5 (G5)	Φ7 (G7)	Gnd	Gnd	Gnd	Gnd
C	0	0	Φ1 (G1)	Φ5 (G5)	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd

CLK (1…8) - output lines of phase selector
CLKG (1…8) – Output lines of glitch generator
Φ(1…8) – Outputs of eight delay cells
G(1…8) – Glitches of eight delay cells

Table 2. Summary of proposed DLL based programmable clock multiplier

Technology	180 nm technology node
Power Supply	1.8 V
DLL Operating Frequency Range	170 MHz – 252 MHz
Charge Pump Current	?80 uA
% Current Mismatch	0.74
Lock Time @ 200 MHz	< 300 ns
Static Phase Error @ 200MHz	?2ps
Frequency Multiplier Frequency Range	170 MHz – 252 MHz (multiply by 1) 340 MHz – 504 MHz (multiply by 2) 680 MHz – 1 GHz (multiply by 4)
Average Power consumption	7.99 mw @ 200 MHz (Fref =200 MHz , 1X) 8.91 mw @ 400 MHz (Fref =200 MHz, 2X) 9.65 mw @ 800 MHz (Fref =200 MHz, 4X)

Table 3. Performance comparison with prior designs

	Power Consumption	Max. Freq.	Vdd	Process	Programmable
[2]	130 mw	900 MHz	3.3 V	0.35 um CMOS	NO
[3]	NA	1.6 GHz	3.3V	0.5 um CMOS	NO
[4]	43 mw	1.1GHz	3.3V	0.35 um CMOS	YES
[5]	23.2 mw	1.2 GHz	2.5V	0.25 um CMOS	YES
[6]	86.6 mw	1.8 GHz	3.3V	0.35 um CMOS	YES
This work	9.65 mw @ 800 MHz	1 GHz	1.8 V	0.18 um CMOS	YES

V.CONCLUSION

The proposed DLL based programmable clock multiplier gives satisfactory results. The DLL can operate for an input frequency range of 170 MHz to 252 MHz without harmonic or false locking and can generate output frequency with multiplication factor of 1X, 2X or 4X depending on the external digital control signals. The output multiplied signal has a duty cycle of exact 50 %. The average power consumption in all the cases is less than 10 mw. The proposed circuit is suitable for various applications in high speed systems due to advantages of low power, fast locking and low static phase error. The idea can be extended to higher multiplication factor by increasing the number of delay cells in VCDL

VI.ACKNOLEDGEMENT

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VII.REFERENCES

[1] B. Kim, T. Weigandt, and P. R. Gray, June-1994 “PLL / DLL System Noise Analysis for Low Jitter Clock Synthesizer Design,” *Intl. Symposium on Circuits and Systems (ISCAS)*,*London* ,vol.4, pp.31-34.

[2] G. Chien and P.Gray, Dec-2000, "A 900 MHz local oscillator using DLL based frequency multiplier technique for PCS applications," *IEEE J. Solid State Circuits*, vol.35, no.12, pp. 1996-1999.

[3] D. J. Foley and M. P. Flynn, Mar.- 2001 "CMOS DLL-based 2-V 3.2-ps jitter 1-GHz clock synthesizer clock synthesizer and temperature-compensated tunable oscillator," *IEEE J. Solid-State Circuits*, vol. 36, pp. 417-423.

[4] C. Kim, I.-C.Hwang, and S.-M. Kang, Nov. -2002 "A low-power small-area +/ 7.28 ps jitter 1 GHz DLL-based clock generator," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1414–1420,.

[5] C. Wang, Y. Tseng, H. She and R. Hu, Dec -2004 " A 1.2 GHz programmable DLL-based frequency multiplier for wireless applications," *IEEE transactions on VLSI systems*, vol. 12, no. 12, pp 1404-1408.

[6] J. Kim, Y. Kwak, M. Kim, S. Kim and C. Kim, Sep-2006. "A 120-MHz–1.8-GHz CMOS DLL-Based Clock Generator for Dynamic Frequency Scaling," IEEE J. Solid State Circuits, vol. 41, no. 9, pp. 2077-2082.

[7] C. Y. Yang and S. I. Liu, Feb.-2001 "A One-Wire Approach for Skew- Compensating Clock Distribution Based on Bidirectional Techniques",*IEEE Journal of Solid-State Circuits*, vol.36, no.6, pp. 266-272.

[8] J. Cheng , Dec-2005 "A Delay-Locked Loop for Multiple Clock Phases/ Delays generation" ,*Ph.D thesis, Georgia Institute of Technology*,.

[9] X. Malliard, F.Devich and M. Kuijk, Jun-2002 "A 900-Mb/s CMOS data recovery DLL using half frequency clock," IEEE J. Solid State Circuit, vol. 37, no. 6, pp. 711-715

[10] Y. Moon, J. Choi, K. Lee, D. K. Jeong and M. K. Kim, Mar.-2000 "An All-Analog Multiphase Delay-Locked Loop Using a Replica Delay Line for Wide-Range Operation and Low-Jitter Performance", *IEEE J. Solid-State Circuits*, vol.35, no.3, pp. 377-384.

[11] W. Lee, J. Cho, S. Lee, 1999 "A High Speed And Low Power Phase Frequency Detector And Charge Pump", *Design Automation Conference , Proc. of the ASP-DAC*, pp. 269-272.

[12] Kun-Seok Lee, Byeong-Ha Park, Han-il Lee, Min Jong Yoh, Sep-2003 "Phase frequency detectors for fast frequency acquisition in zero-dead-zone CPPLLs for mobile communication systems",*IEEE, ESSCIRC '03.Proceedings of the 29th European* , pp 525-528 .

[13] R. Chang and L. Kuo, May-2000, "A New Low Voltage Charge Pump Circuit For PLL*", IEEE int. symposium on Circuits And Systems,* Geneva, pp. v701-v704.

[14] M. G. Johnson and E. L. Hudson, Oct.-1988 "A variable delay line PLL for CPU-coprocessor synchronization," *IEEE J. Solid-State Circuits*, vol. 23, pp.1218-1223.

[15] K.H. Chen and Y Lo, Sep. 2004,"A Fast-Lock DLL with Power-On Reset Circuit," *IEICE Trans. on Fundamentals*, Vol.E87-A No.9, pp.2210-2220.

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